Please amend the paragraph on page 10, lines 20-26, as follows:

A2

The interconnect layer 22 is a stacked layer including, for example, a silicon layer and a metal silicide layer laid on the silicon layer. The layer 22 may include a silicon-germanium alloy layer and a metal silicide layer lying on the silicon-germanium alloy layer. The upper-surface region of the gate electrode 18 may be a silicide layer.

Please amend the paragraph on page 17, lines 7-14, as follows:

A3

In FIG. 6, there is illustrated, in perspective view, part of a semiconductor device according to a second embodiment of the present invention. The second embodiment differs only in part from the first embodiment. In FIG. 6, therefore, parts corresponding to those in FIG. 3 are denoted by like reference numerals, and descriptions thereof are omitted. Only the differences from FIG. 3 will be described below.

Please amend the paragraph bridging pages 22 and 23, as follows:

A4

FIG. 8 illustrates, in perspective view, part of a semiconductor device according to a third embodiment of the present invention. The third embodiment differs only in part from the second embodiment shown in FIG. 6. In FIG. 8, therefore, parts corresponding to those in FIG. 6 are denoted by like reference numerals and descriptions thereof are omitted. Only the differences from FIG. 6 will be described below.

Please amend the paragraph bridging pages 28 and 29, as follows:

A5

FIG. 10 illustrates, in perspective view, part of a semiconductor device according to a fourth embodiment of the present invention. The fourth embodiment differs only in part from the third embodiment shown in FIG. 8. In FIG. 10, therefore, parts corresponding to those in